

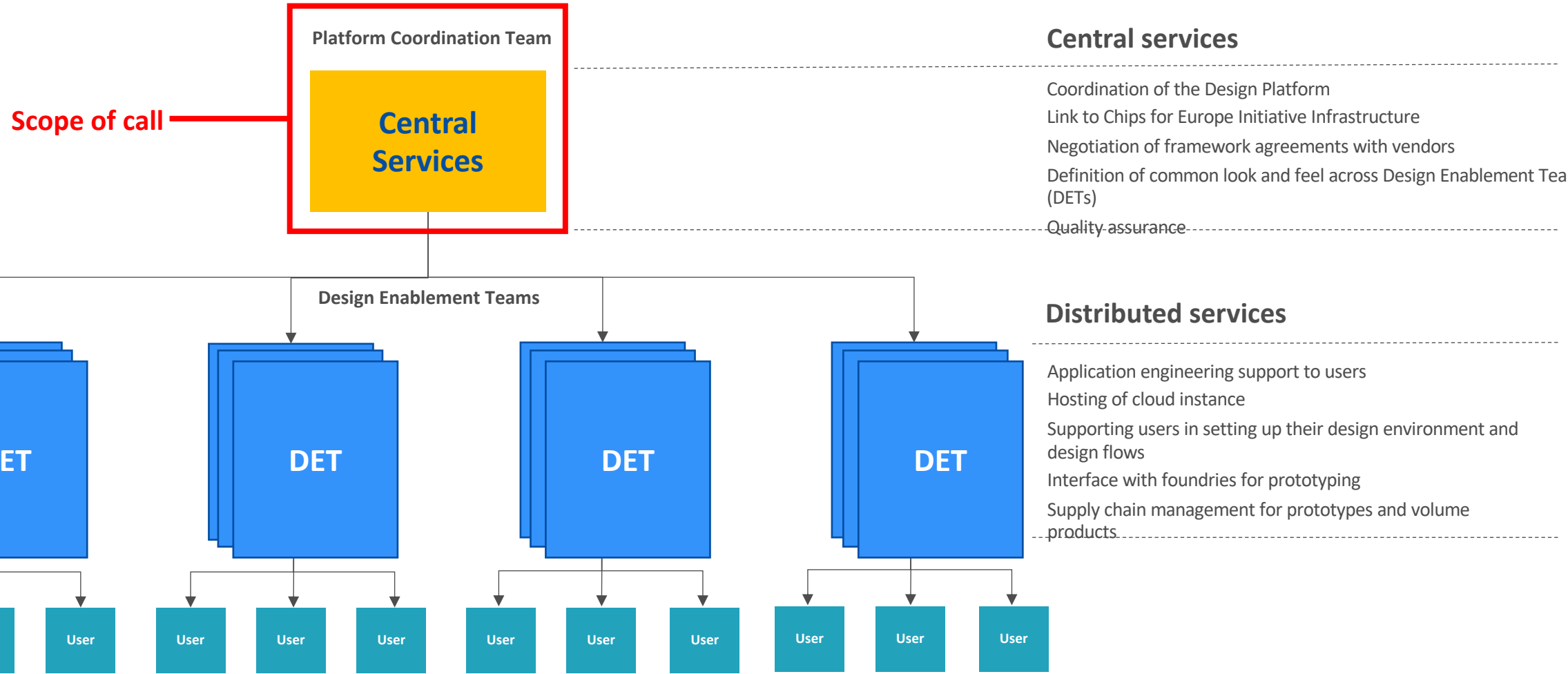


# Call for Design Platform

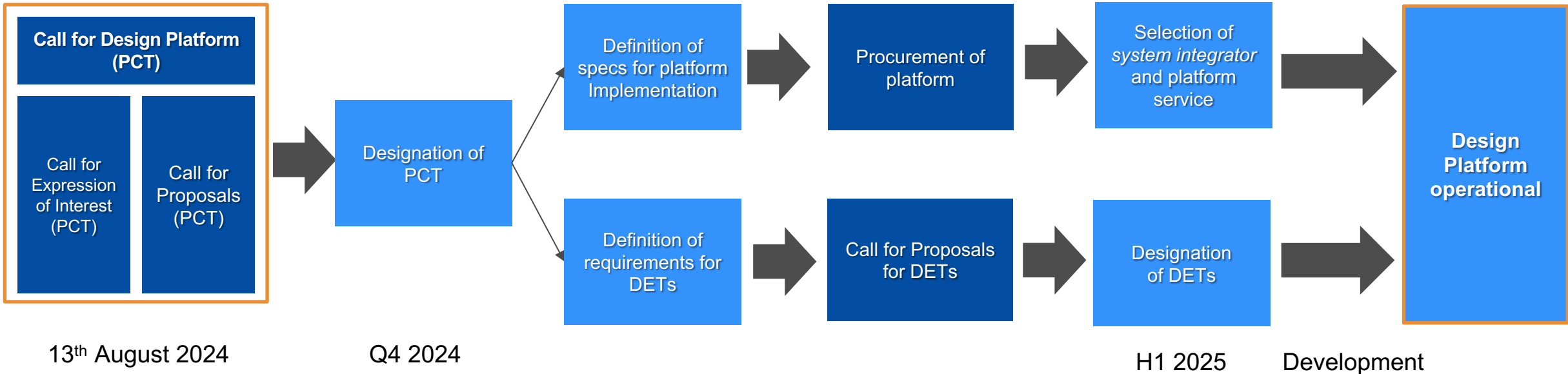
Chips JU Info Session - 11 July 2024

*Microelectronics and Photonics Industry Unit - DG CNECT*

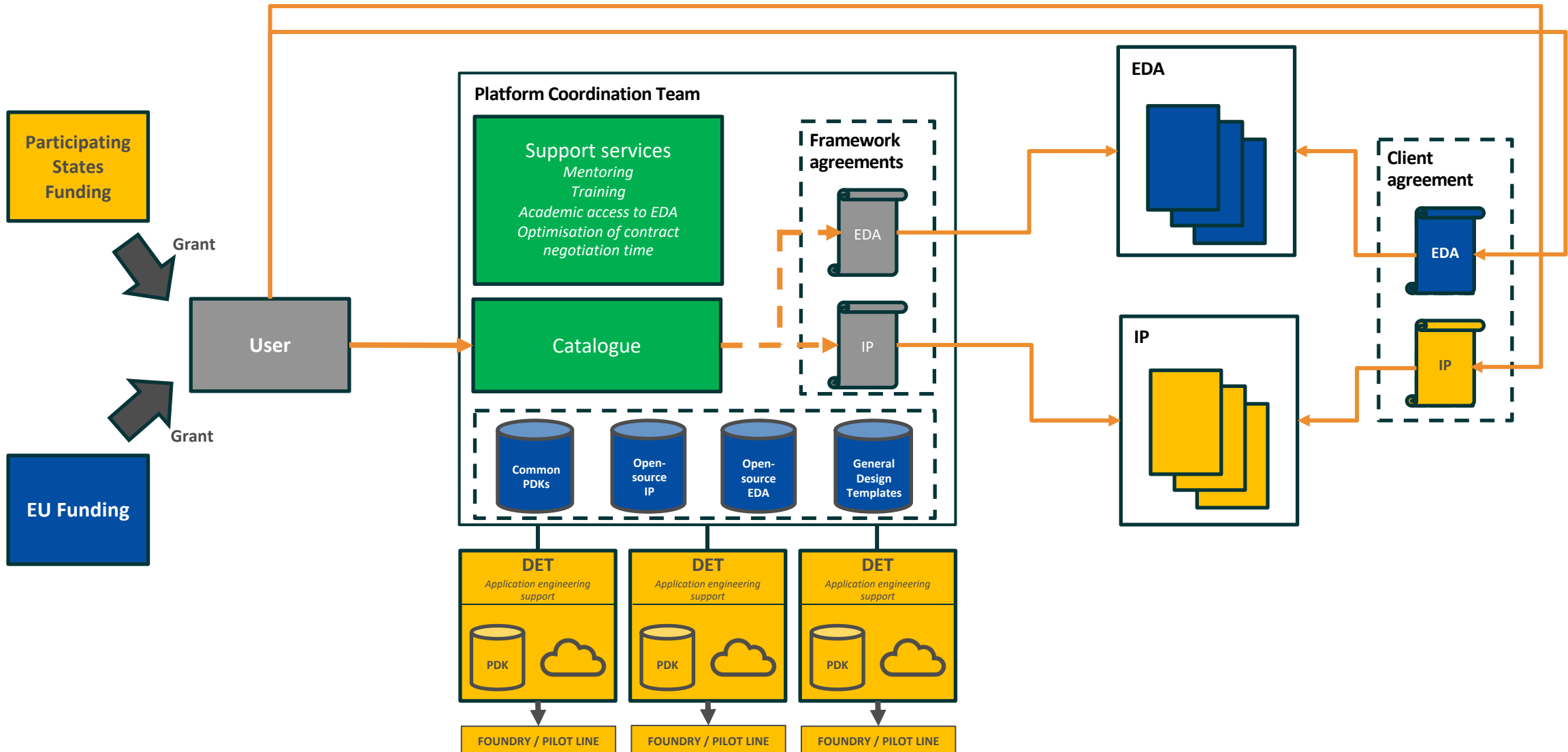
# Design Platform Architecture



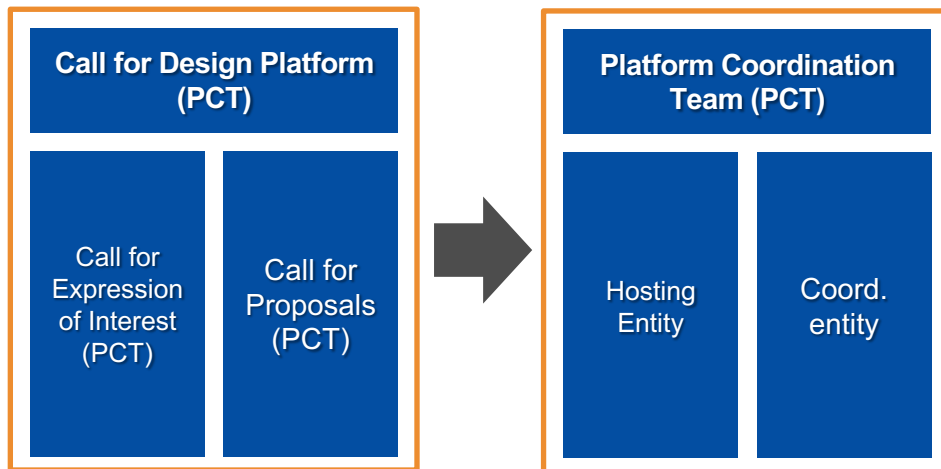
JU



# Conceptual Architecture for the Design Platform



# Role of PCT



Coordinating entity of the Design Platform (CSA call)

- Digital Europe CSA call - results in a **grant agreement** and the selection of the consortium that will manage the Design Platform as the PCT.

Hosting consortium for the cloud service

- Call for Expression of Interest – results in a hosting agreement and the selection of a hosting consortium to manage the cloud service that will be **procured by the Chips JU**.

# Design platform – user funnel

## Design Platform – Startup support

### Level 1 service

#### Incubation stage

*Licenses at nominal fee*

Up to PoC - TRL3



#### Selection Procedure

*Managed by PCT*

Technical proposal  
Proof-of-concept  
Business plan

Expert  
evaluation

Selection

### Level 2 service

#### Acceleration stage

*Partial license cost funding*

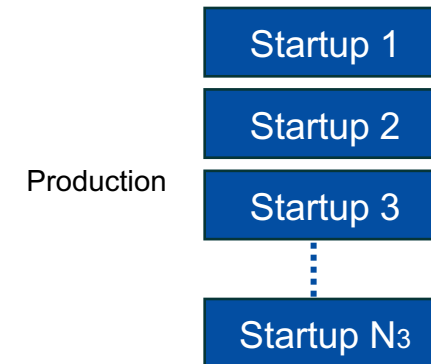
Up to TRL 8



### Commercial stage

*No EC funding*

TRL 9\*



Production

*PCT grants  
access to  
eligible  
startups*

PCT operates for startups similarly to Europractice for academia:

- framework agreement
- managed licensing at incubator level
- direct startup license at pre-comm level

# Call text structure

- General call information
  - Call plan, budget and provisions
- Technical description
- Implementation
- Application criteria
  - Admissibility, Eligibility, Exclusion, Evaluation
- Process
  - Submission, Evaluation, planning
- Annexes

# General access conditions



Availability



Transparency



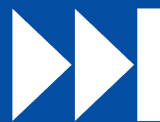
Non-discrimination



Proportionality



Market Terms



Preferential Access  
for start-ups and SMEs



Fairness



International  
Partnerships

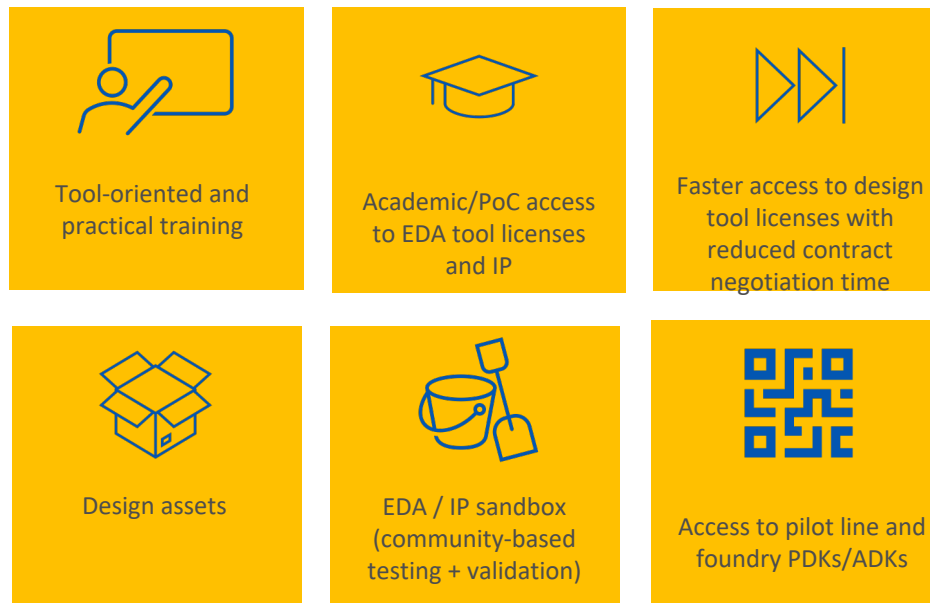
# General access conditions

- Access to the Design Platform should be based on fair and non-discriminatory principles and should be limited to Participating States of the Chips JU.
- In determining access to the Design Platform for users established in any Participating State but controlled from third countries that are not Participating States of the Chips JU, consortia must take into consideration the following two main criteria:
  - **EU added value**, i.e., their contribution to the objectives of the Chips Act as set out in Article 4.
  - **Economic security considerations.**
- Only users from organisations that can clearly demonstrate their contribution to EU added value, their alignment with European economic security shall be granted access. Users from third countries will be granted access when this is foreseen in the international obligations of the Union concerning semiconductors, as these defined in any relevant Digital Partnerships or Trade and Technology Council agreements.

# Implementation of support programme

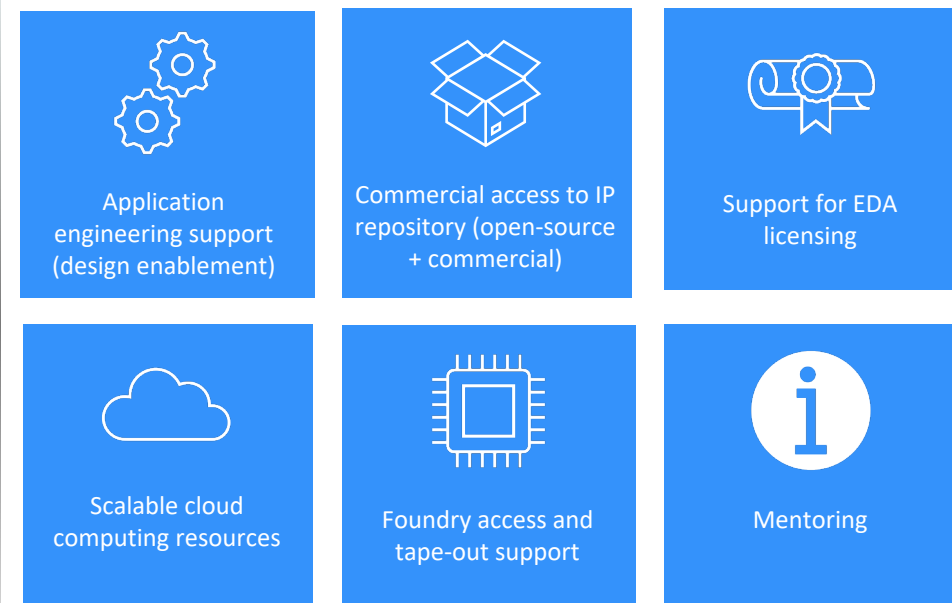
## Design Platform Services

### Level 1



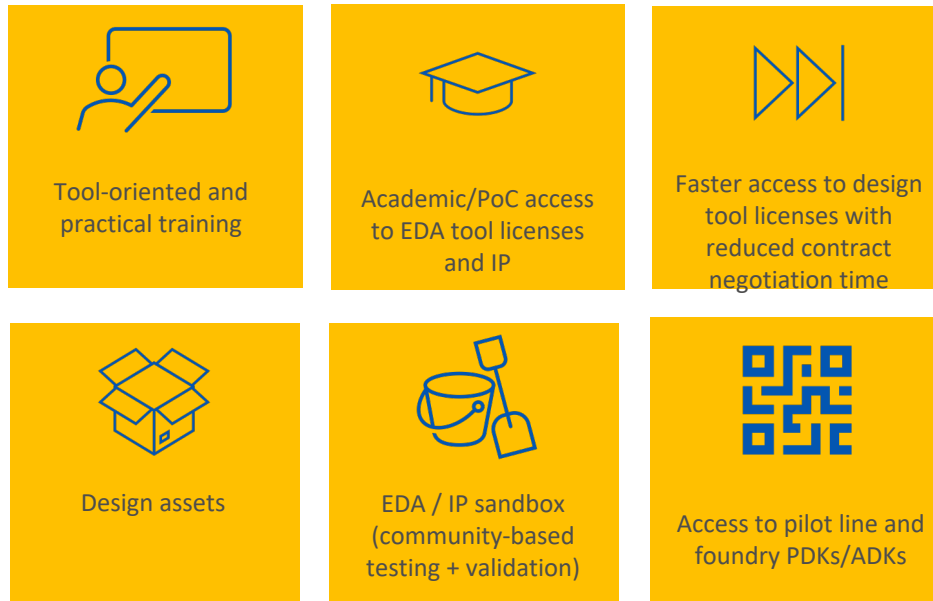
Access open to qualified designers from entities (commercial and non-) based in EU or 'Chips JU' PS

### Level 2



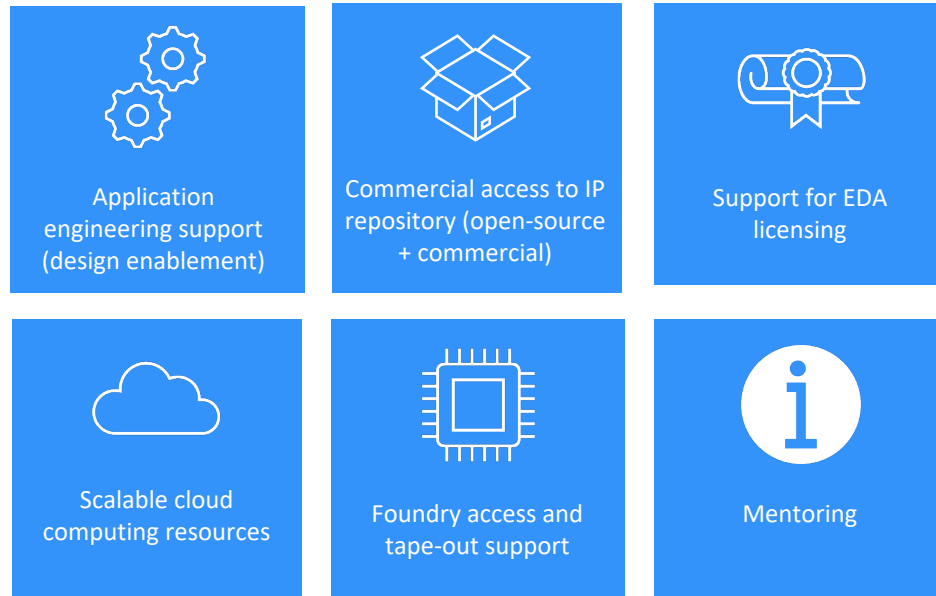
Market rates or access to selected entities with support granted by EU + PS of 'Chips JU'

# Access to Level 1 services



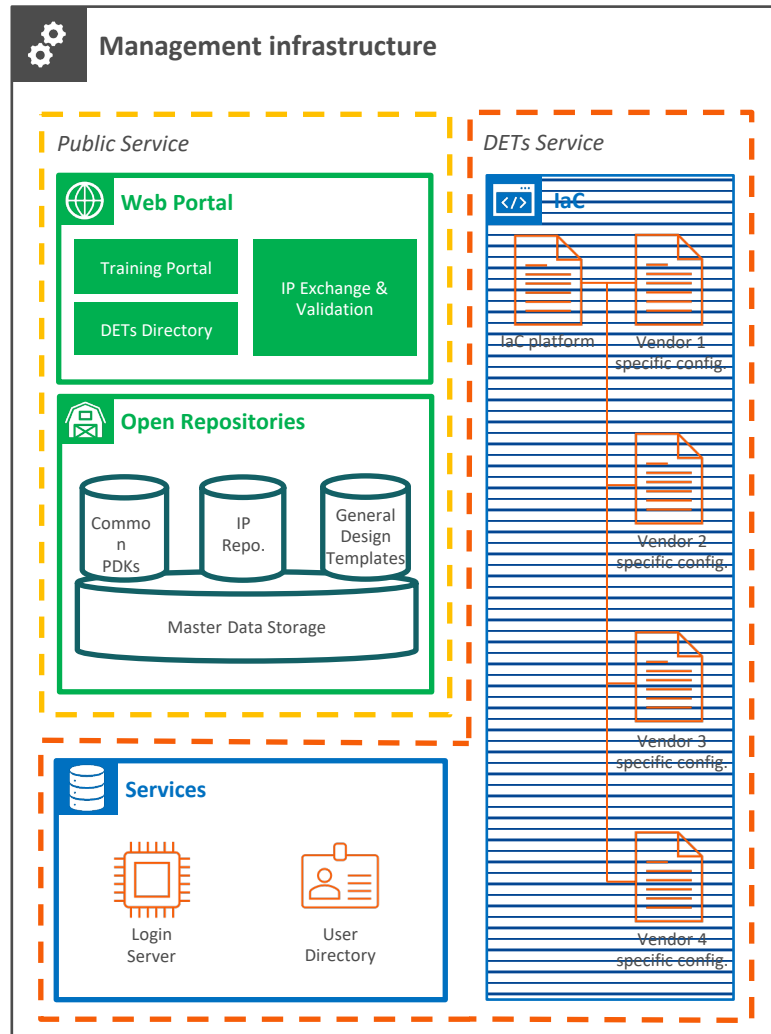
- These services should be open to **all users in the EU who satisfy some basic eligibility criteria** to be proposed by the applying PCT consortia.
- Should be accessible to all legal entities from Chips JU Participating States against market terms **with highly reduced or zero prices and preferential access for start-ups and SMEs.**
- For those legal entities established in Participating States but controlled from third countries, the access conditions are subject to the general access conditions (on int. partnerships).

# Access to Level 2 services



- Potentially access via **potential financial support** from the Union and Participating States. Otherwise companies may get access to these services **via market prices**.
- Access for legal entities established in Participating States but controlled from third countries shall be determined based on **EU added value and economic security**.

# PCT Cloud service



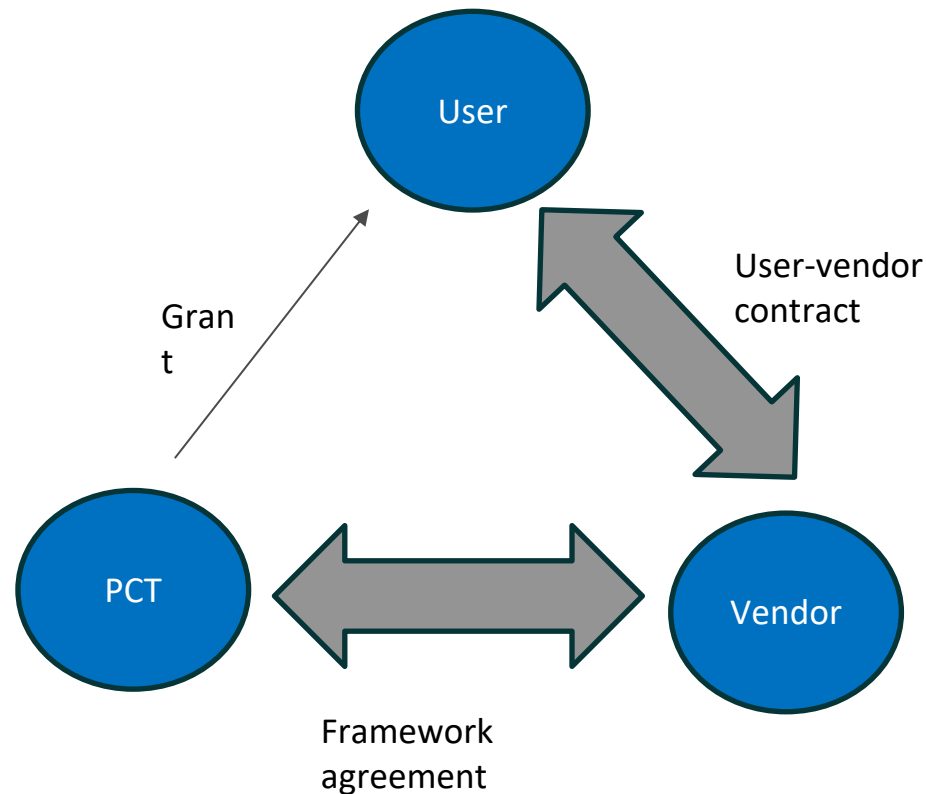
**Web portal** with **training** resources, **IP/tool exchange**, and service provider directory.

**Common repositories** for European project IPs, PDKs/ADKs from Chips for Europe or Horizon Europe, and design templates.

**Templates of virtual machines** or containers containing all the software components and configuration, as well as **Infrastructure as Code** required to operate a given electronic design software, and that can be easily deployed on the cloud instances operated by the DETs.

**User authentication** system with login server, directory, and security features.

# Potential acquisition model of 'Level 2' EDA Tools



- PCT should negotiate a framework agreement with the EDA vendor setting out conditions and capped rates for EDA licensing depending on a company's funding and the type of development (digital, mixed signal, analogue).
- For Level 2 users, once the vendor and the user reach an agreement on the tools that will be acquired, part of the costs could be re-funded by a grant.

# Expected outcomes (1)

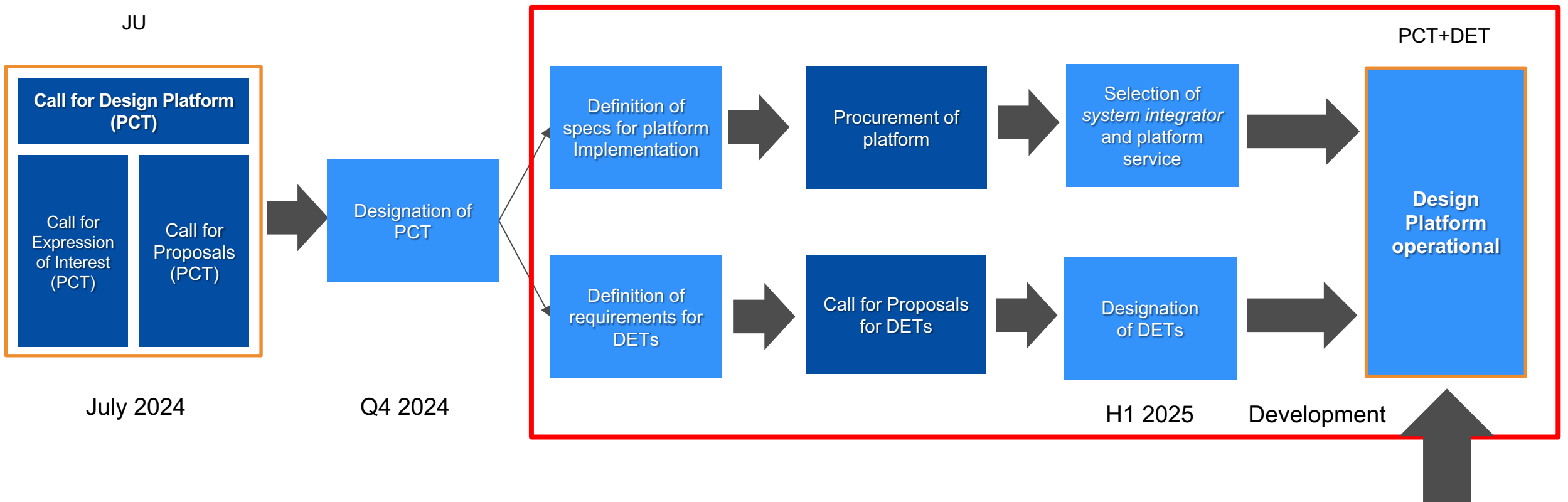
- Easy **cloud-enabled access to electronic design tools** (including proprietary and open-source tools), **libraries of design templates**, as well as **training and support services**, accelerating chip design and reducing time-to-market for users.
- The cloud services, procured by the Chips JU, may be developed and maintained by third parties, however the **PCT, in line with a Hosting Agreement**, shall assume responsibility for the **coordination** and **execution** of the various related activities and services described below.
- The PCT shall **oversee** that the **cloud service procured** by the Chips JU is secure, scalable, and accessible 24/7.
- The PCT shall continuously **monitor the operation** of the Design Platform and the **quality of services provided to users**. This includes incorporating user feedback loops and adopting corrective measures as necessary.

## Expected outcomes (2)

- The **management and maintenance of a cloud-based repository** for the European chip design community, populated with an extensive portfolio of open-source and proprietary 'design assets'.
- A quicker and more efficient **licensing process** for commercial EDA tools and IP libraries, reducing burden and barriers for companies engaging in chip design, coupled with a startup support programme, that includes financing of licensing costs.
- Integration in the Design Platform of **Design Enablement Teams**, that will be designated following a subsequent linked call.
- **Advanced training and support services** available to a wide range of users via the Design Platform **complementing the work of the network of Competence Centres** and/or potential future dedicated actions on design skills to support the development of design skills across the Union.
- A **start-up & SME** support programme.

# Next steps

JU



**Start-up/SME support scheme launches..**

# Thank you



© European Union 2024

Unless otherwise noted the reuse of this presentation is authorised under the [CC BY 4.0](#) license. For any use or reproduction of elements that are not owned by the EU, permission may need to be sought directly from the respective right holders.